CLAIMS

We claim:

1. An electrical interconnection structure for connection to large electrical contacts comprising:

a semiconductor substrate having a conductive pad layer formed thereon;

a dielectric layer overlying the conductive pad layer, the dielectric layer having formed therein a plurality of elongate trenches that extend into the dielectric layer such that electrical connections to the underlying conductive pad layer can be formed; and

a plurality of elongate conductive contacts formed in the elongate trenches to establish electrical connections to the underlying conductive pad layer.

2. The electrical interconnection structure of Claim 1 wherein a top portion of the elongate conductive contacts are electrically connected to other circuit elements.

3. The electrical interconnection structure of Claim 1 wherein the conductive pad layer is formed of a copper-containing material; and

wherein the elongate conductive contacts are formed of a copper-containing material.

4. The electrical interconnection structure of Claim 3 wherein the conductive pad layer includes a plurality of elongate slots that extend through the conductive pad layer to expose the underlying semiconductor substrate, the slots having a long axis, a short axis, and having sidewalls;

wherein the plurality of elongate trenches in the dielectric layer have a long axis and a short axis and wherein the trenches are configured such that the long axes of the trenches lie transverse to the long axes of the elongate slots in the conductive pad layer; and

wherein the elongate conductive contacts can be electrically connected to the pad layer through slot sidewalls of the pad layer.

5. The electrical interconnection structure of Claim 4 wherein the plurality of elongate trenches in the dielectric layer extend downward to the exposed semiconductor substrate in regions where said trenches overlie the elongate slots in the conductive pad layer; and

wherein the elongate conductive contacts that are formed in the plurality of elongate trenches extend down to the exposed underlying semiconductor substrate and down to the underlying conductive pad layer to establish electrical connections to the underlying conductive pad layer.

6. The electrical interconnection structure of Claim 3 wherein the conductive pad layer includes a plurality of elongate slots that extend through the conductive pad layer to expose the underlying semiconductor substrate, the slots having a long axis, a short axis, and sidewalls;

wherein the plurality of elongate trenches in the dielectric layer have a long axis and a short axis and wherein the elongate trenches are configured such that the long axis of the elongate trenches in the dielectric layer lie substantially parallel to the long axis of the elongate slots in the conductive pad layer.

7. The electrical interconnection structure of Claim 6 wherein the plurality of elongate trenches in the dielectric layer extend downward to the exposed semiconductor substrate in regions where said trenches overlie the elongate slots in the conductive pad layer.

8. The electrical interconnection structure of Claim 6 wherein the plurality of elongate trenches in the dielectric layer extend downward to the exposed semiconductor substrate in regions where said trenches overlie the elongate slots such that the elongate conductive contacts can be electrically connected to the pad layer through slot sidewalls of the pad layer.

9. An electrical interconnection structure for connection to large electrical contacts comprising:

a semiconductor substrate having a copper pad formed thereon, the copper pad includes a plurality of elongate slots that extend into the pad to expose a portion of the underlying substrate such that the substrate is exposed, the elongate slots each including a long axis, a short axis, and sidewalls;

a dielectric layer overlying the copper pad, the dielectric layer including a plurality of elongate bar trenches that extend into the dielectric layer such that electrical connections to the underlying conductive pad layer can be formed, the bar trenches including a long axis and a short axis; and

a plurality of elongate conductive contacts that are formed in the plurality of elongate trenches establishing electrical connections to the underlying conductive pad layer.

10. The electrical interconnection structure of Claim 9 wherein the elongate conductive contacts are electrically connected to the sidewalls of the copper pads.

11. The electrical interconnection structure of Claim 10 wherein the long axes of the plurality of elongate bar trenches are arranged to be substantially parallel to the long axes of the plurality of elongate slots formed in the copper pad.

12. The electrical interconnection structure of Claim 11 wherein the elongate conductive contacts include copper material.

13. The electrical interconnection structure of Claim 12 wherein the elongate conductive contacts include at least one barrier layer.

14. The electrical interconnection structure of Claim 11 wherein a top portion of the elongate conductive contacts are electrically connected to other circuit elements.

15. The electrical interconnection structure of Claim 10 wherein the long axes of the plurality of elongate bar trenches are arranged transversely to the long axes of the plurality of elongate slots formed in the copper pad.

16. The electrical interconnection structure of Claim 15 wherein the elongate conductive contacts include copper material.

17. The electrical interconnection structure of Claim 16 wherein the elongate conductive contacts include at least one barrier layer.

18. The electrical interconnection structure of Claim 15 wherein a top portion of the elongate conductive contacts are electrically connected to other circuit elements.

19. A method for forming an electrical interconnection structure for connection to large electrical contacts, the method comprising:

providing a semiconductor substrate having a copper-containing pad layer formed thereon such that the copper-containing pad layer includes a plurality of elongate slots having a long axis, a short axis, and sidewalls, the slots extending through the pad layer to expose the underlying semiconductor substrate;

forming, over the pad layer, a dielectric layer having a plurality of elongate trenches formed therein, the elongate openings having a long axis, a short axis, and sidewalls and are configured to extend into the dielectric layer to a depth such that electrical connections to the underlying copper-containing pad layer can be formed;

forming elongate copper-containing contacts in the plurality of elongate openings thereby establishing electrical connections to the underlying copper-containing pad layer; and

conducting further processing as needed.

20. A method as in Claim 19 wherein the step of forming the dielectric layer comprises forming the dielectric layer such that the long axis of the elongate slots lies substantially parallel to the long axis of the elongate trenches in the pad layer to expose a portion of the sidewalls of the elongate trenches of the pad layer.

21. A method as in Claim 20 wherein the step of forming elongate copper-containing contacts in the plurality of elongate trenches includes the steps of:

forming at least one barrier layer in the elongate slots;

forming a seed layer in the elongate slots;

forming a bulk copper-containing layer on the seed layer; and

wherein the step of conducting further processing includes removing excess copper-containing materials from a surface of the dielectric layer and electrically connecting the elongate copper-containing contacts to other circuit elements.

22. A method as in Claim 21 wherein the step of conducting further processing includes forming other semiconductor circuit structures.

23. A method as in Claim 19 wherein the step of forming the dielectric layer comprises forming the dielectric layer such that the long axis of the elongate slots lies transverse to the long axis of the elongate trenches in the pad layer to expose a portion of the sidewalls of the elongate trenches of the pad layer.

24. A method as in Claim 23 wherein the step of forming elongate copper-containing contacts in the plurality of elongate trenches includes the steps of:

forming at least one barrier layer in the elongate slots;

forming a seed layer in the elongate slots;

forming a bulk copper-containing layer on the seed layer; and

wherein the step of conducting further processing includes removing excess copper-containing materials from a surface of the dielectric layer and electrically connecting the elongate copper-containing contacts to other circuit elements.

25. A method as in Claim 24 wherein the step of conducting further processing includes forming other semiconductor circuit structures.